REQUIREMENTS-BASED UVM VERIFICATION AND TRACEABILITY

CHALLENGE

With the increasing complexity of electronic systems that feature a closer interaction between embedded software, hardware and analog components, the verification and traceability of tests at requirement level has become mission-critical.

Evaluating the requirements coverage, assessing the impact of a change request on tests, identifying non-regression test suites have to be carried out as early as possible in the design lifecycle.

BENEFITS

- Capability to debug the hardware/software system before the availability of the hardware prototype
- Full traceability of test requirements: impact analysis of change requests, creation of links between fragments and IP-XACT elements [More...]

SOLUTIONS

Magillem verification tools provide the environment for a verification flow that enables to automate the creation of a test bench.
Test cases are captured at specification level, all UVCs (Universal Verification Components) are described in the IP-XACT standard format.
The tool selects the UVCs and generates the full SystemC AMS test bench [More...]

RELATED RESOURCES

- Flyer Magillem: Requirement based UVM Verification and Traceability
- Paper DVCon Europe 2014 : Generation of UVM compliant Test Benches for Automotive... [More...]

Contact us for more information